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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,265	04/25/2001	Joe Bolding	10010394-1	9776

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EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	**PAPER NUMBER**
2114	2

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,265	BOLDING ET AL.	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-14 and 16-20* is/are rejected.

7)☒ Claim(s) *4-8,15 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Bissett, et al, U.S. Patent Number 6,279,119. Regarding claim 1:

a. Regarding the limitation of "providing a synchronous breakpoint at a predetermined address location with respect to said code portion," Bissett discloses a system with an interrupt that can be performed after a fixed amount of clock cycles. (Lines 43-45 of Column 3). Bissett also disclose that a breakpoint may be generated after a fixed number of instructions. (Lines 45-47 of Column 3).

b. Regarding the limitation of "executing said code portion on said processors in said simulated multiprocessor environment from a fixed location," Bissett discloses a system wherein compute elements can be configured to refresh operation to synchronize execution of operation. (Lines 26-30 of Column 3).

c. Regarding the limitation of "when a first processor of said processors encounters said synchronous breakpoint, terminating execution of said code portion on said first processor while continuing to execute said code portion on remaining processors," Bissett discloses a system wherein processing can be aligned by the interrupts. (Lines 53-59 of

Column 3). Bissett discloses that interrupts maybe generated after a fixed number of instructions. (Lines 45-47 of Column 3).

3. Regarding claim 2, Bissett discloses a system with wherein the interrupt serves to align the processing by the computer elements with the clocking structure. (Lines 55-57 of Column 3). Bissett also discloses that repair can be initiated by a user upon detection of a failure. (Lines 25-26 of Column 7).

4. Regarding claim 3, Bissett discloses a system wherein a primary processor and have an interrupt and upon being generated cause a synchronous interrupt to all secondary processor to occur. (Lines 40-52 of Column 3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10-14 and 16-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Ghameshlu, et al, U.S. Patent Number 6,694,449 and in further view of Bissett, et al, U.S. Patent Number 6,279,119.

7. Regarding claim 10:

d. Regarding the limitation of "providing an architectural simulator operable to simulate said target hardware platform, said architectural simulator having a debugger associated therewith, wherein said target hardware platform comprises a multiprocessor

system," Ghameshlu discloses a system with a multiprocessor environment (Lines 15-17 of Column 8), with an error diagnosis in the processor.

e. Regarding the limitation of "initializing in said architectural simulator a list of processors included in said target hardware platform," Ghameshlu discloses a system with a multiple processor devices and Ghameshlu discloses a crossover bus connects at least one further processor device to the first process, in which signature data is passed over the bus. Ghameshlu does not disclose a system with a list of processors in the target hardware. Bissett discloses a multiple processor system that stores a configuration list of processors operating normally. (Lines 65-67 of Column 6). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the art of Ghameshlu and Bissett. One of ordinary skill would have been inclined to combine the art because Ghameshlu discloses a need for a way to store signature information received over the crossover bus wherein the signature passed over the passed in check with a stored signature for error handling. (Lines 60-67 of Column 3 and Lines 1-4 of Column 4). Bissett disclose a system in which a configuration list is maintained for the transmission of the state information of the processor. (Lines 65-67 of Column 6 and Lines 1-2 of Column 7).

f. Regarding the limitation of "setting a synchronous breakpoint at a predetermined address location with respect to said code portion operable to be executed on said architectural simulator," Bissett discloses a system with an interrupt that can be performed after a fixed amount of clock cycles. (Lines 43-46 of Column 3).

g. Regarding the limitation of "launching said code portion on said architectural simulator from a fixed location," Ghameshlu discloses a system with a comparer to receive data and launches an error handling program. (Lines 18-20 of Column 4).

h. Regarding the limitation of "automatically stepping through said list of processors until each of said processors of said architectural simulator reaches said synchronous breakpoint," Ghameshlu discloses a system with the ability to continue operation in the processor system on the remaining processor to achieve a frictionless continuation of the operations being processed. (Lines 25-33 of Column 6).

i. Regarding the limitation of "returning program control to said debugger for performing a debug operation," Ghameshlu discloses a system with an error diagnosis that triggers error handling. (Lines 20-22 of Column 4).

8. Regarding claim 11, Bissett discloses an SMP system. (Lines 11-13 of Column 3).

9. Regarding claim 12, Ghameshlu discloses an asymmetrical system by disclosing two separate processors. (See Figure 1).

10. Regarding claim 13, Bissett disclose a system wherein the processor asynchronous to each other. (Lines 49-51 of Column 7).

11. Regarding claim 14, Ghameshlu discloses a system in which the processors are duplicated processors that perform same operations and are direction coupled together. (Lines 39-45 of Column 3).

12. Regarding claim 16:

j. Regarding the limitation of "providing an architectural simulator operable to simulate said target hardware platform, said architectural simulator having a debugger

associated therewith, wherein said target hardware platform comprises a multiprocessor system," Ghameshlu discloses a system with a multiprocessor environment (Lines 15-17 of Column 8), with an error diagnosis in the processor.

k. Regarding the limitation of "initializing in said architectural simulator a list of processors included in said target hardware platform," Ghameshlu discloses a system with a multiple processor devices and Ghameshlu discloses a crossover bus connects at least one further processor device to the first process, in which signature data is passed over the bus. Ghameshlu does not disclose a system with a list of processors in the target hardware. Bissett discloses a multiple processor system that stores a configuration list of processors operating normally. (Lines 65-67 of Column 6). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the art of Ghameshlu and Bissett. One of ordinary skill would have been inclined to combine the art because Ghameshlu discloses a need for a way to store signature information received over the crossover bus wherein the signature passed over the passed in check with a stored signature for error handling. (Lines 60-67 of Column 3 and Lines 1-4 of Column 4). Bissett disclose a system in which a configuration list is maintained for the transmission of the state information of the processor. (Lines 65-67 of Column 6 and Lines 1-2 of Column 7).

l. Regarding the limitation of "setting a synchronous breakpoint at a predetermined address location with respect to said code portion operable to be executed on said architectural simulator," Bissett discloses a system with an interrupt that can be performed after a fixed amount of clock cycles. (Lines 43-46 of Column 3).

m. Regarding the limitation of "launching said code portion on said architectural simulator from a fixed location," Ghameshlu discloses a system with a comparer to receive data and launches an error handling program. (Lines 18-20 of Column 4).

n. Regarding the limitation of "automatically stepping through said list of processors until each of said processors of said architectural simulator reaches said synchronous breakpoint," Ghameshlu discloses a system with the ability to continue operation in the processor system on the remaining processor to achieve a frictionless continuation of the operations being processed. (Lines 25-33 of Column 6).

o. Regarding the limitation of "returning program control to said debugger for performing a debug operation," Ghameshlu discloses a system with an error diagnosis that triggers error handling. (Lines 20-22 of Column 4).

13. Regarding claim 17, Bissett discloses an SMP system. (Lines 11-13 of Column 3).

14. Regarding claim 18, Ghameshlu discloses an asymmetrical system by disclosing two separate processors. (See Figure 1).

15. Regarding claim 19, Bissett disclose a system wherein the processor asynchronous to each other. (Lines 49-51 of Column 7).

16. Regarding claim 20, Ghameshlu discloses a system in which the processors are duplicated processors that perform same operations and are direction coupled together. (Lines 39-45 of Column 3).

17. Claim 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bissett as applied to claim 1 above, and further in view of Ghameshlu, et al, U.S. Patent Number 6,694,449.

18. Regarding claim 8, Bissett discloses a multiprocessor system with the ability to synchronize break points. Bissett does not disclose a system wherein the debugger program is integrated. Ghameshlu disclose a system with an error handler in the processor device. (Lines 20-22 of Column 4). Ghameshlu also disclose a system with an debugging enabled during servicing of the system. (Lines 31-34 of Column 4 and Lines 59-67 of Column 16). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the art of Ghameshlu and Bissett. One of ordinary skill would have been inclined to combine the art because Bissett discloses a fault tolerant computer system however no error handling is disclosed. Ghameshlu discloses a way to handle and diagnose the faults. (Lines 20-22 of Column 4).

19. Regarding claim 9, Bissett discloses a multiprocessor system with the ability to synchronize break points. Bissett does not disclose a system wherein the debugger program is integrated. Ghameshlu disclose a system with an error handler in the processor device. (Lines 20-22 of Column 4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the art of Ghameshlu and Bissett. One of ordinary skill would have been inclined to combine the art because Bissett discloses a fault tolerant computer system however no error handling is disclosed. Ghameshlu discloses a way to handle and diagnose the faults. (Lines 20-22 of Column 4).

Allowable Subject Matter

20. Claims 4-7, 15, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 7:30-5:00, every other Friday off**. The examiner can be reached at: **703-305-7762**.

22. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Rob Beausoliel.**

- The supervisor can be reached on **703-305-9713.**

23. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

25. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **703-305-3900.**

26. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

Tim Bonura
Examiner
Art Unit 2114

NADEEM IQBAL
PRIMARY EXAMINER

tmb
May 29, 2004